29. (Amended) The restraint system of claim 25, wherein the sensing circuit is coupled to provide a signal having a fractional pulse density that is indicative of acceleration.

Remarks:

A. Amendment of Claims

Claims 1-9, 20-22 and 26-29 have been amended to improve clarity. More so claim 9 has been amended to overcome the objection to the informality raised by the Office Action.

B. Objection to Claim 9

Claim 9 was objected to for an informality. It is respectfully submitted that the amendment to claim 9 to indicate that the claimed first and second capacitors are the same as set forth in claim 8, overcomes the objection to claim 9. Accordingly, Applicants respectfully request the objection to be withdrawn.

C. Rejection of Claims 1-6, 8-9, 11-14 and 19-22 Under 35 U.S.C. § 102(b)

Pending claims 1-6, 8, 9, 11-14 and 19-22 stand rejected under § 102(b) as being anticipated by U.S. Patent No. 4,642,555 (Swartz). Applicants respectfully traverse the rejection. With respect to claim 1, Swartz does not disclose an input block to apply an input signal to a common input terminal of a sensing block. In this regard, Swartz does not disclose a sensing block having a common input terminal. The positive voltage node referred to by the Office Action (See Office Action, p. 2) is applied to, respectively, different resistors 1 and 4 and neither it, nor anything else in Swartz is a common input terminal. For at least this reason, claim 1 and claims 2-6 and

8-9 depending therefrom are patentable over Swartz. For similar reasons claims 11-14 are also patentable.

With respect to claim 19, nowhere does Swartz disclose an input block to provide an input signal to a common terminal of a first capacitor and a second capacitor of a sensing block. In this regard, in Swartz there is no common terminal of the first capacitor and the second capacitor that is provided an input signal. Accordingly, claim 19 and claims 20-22 depending therefrom are patentable.

D. Rejection of Claims 10 and 23-30 Under 35 U.S.C. § 103(a)

Pending claims 10 and 23-30 stand rejected under 35 U.S.C. § 103(a) over Swartz in view of U.S. Patent No. 5,528,520 (Kemp). Because neither Swartz or Kemp teach or suggest application of an input signal to a common input terminal of a sensing block, claim 10 and claims 25-30 are patentable over the proposed combination. Nor does either Swartz or Kemp teach or suggest an input signal provided to a common terminal of a first capacitor and a second capacitor of a sensing block as recited by claim 19. Thus for at least this reason, claims 23 and 24 (which depend from claim 19) are also patentable over the proposed combination.

E. Allowable Subject Matter

Applicants gratefully acknowledge the indication that claims 7 and 15-18 would be allowable if rewritten in independent form. However in light of the above remarks, it is respectfully submitted that claims 1 and 11 from which claims 7 and 15-18 depend are also patentable and therefore claims 7 and 15-18 are patentable in their present form.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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APPENDIX

1. (Amended) An apparatus comprising:

an input block to apply an input signal to a common input terminal of a sensing block; and

a converting block to receive a sensed signal from a sensing block in response to [applying] the input signal.

2. (Amended) The apparatus of claim 1, wherein the converting block is coupled to [provides] provide an output signal based on the sensed signal.

3. (Amended) The apparatus of claim 1, wherein the converting block is coupled to [provides] provide a signal having a fractional pulse density that is indicative of acceleration.

4. (Amended) The apparatus of claim 1, wherein the input block is coupled to [applies] apply a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

5. (Amended) The apparatus of claim 1, wherein the converting block is configured to [integrates] integrate the sensed signal and [provides] provide a first output signal and a second output signal.

6. (Amended) The apparatus of claim 5, wherein the converting block is further configured to [compares] compare the first output signal and the second output signal and [provides] provide an output signal.

7. (Amended) The apparatus of claim 6, wherein the converting block is coupled to [provides] provide the output signal to the input block.

8. (Amended) The apparatus of claim 1, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to [provides] provide a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

9. (Amended) The apparatus of claim 8, wherein the input block is coupled to [provides] provide the first input signal through the [a] first capacitor and the second input signal through the [a] second capacitor.

20. (Amended) The apparatus of claim 19, wherein the converting block is coupled to [provides] provide a digital signal based on the sensed signal.

21. (Amended) The apparatus of claim 19, wherein the input block is coupled to [applies] apply a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

22. (Amended) The apparatus of claim 19, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to [provides] provide a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

26. (Amended) The restraint system of claim 25, wherein the deployment block is coupled to [provides] provide the activation signal to activate an airbag.

27. (Amended) The restraint system of claim 25, wherein the sensing circuit is coupled to be clocked [using] via a plurality of non-overlapping clocks.

28. (Amended) The restraint system of claim 25, wherein the sensing circuit is configured to [provides] provide a digital signal.

29. (Amended) The restraint system of claim 25, wherein the sensing circuit is coupled to [provides] provide a signal having a fractional pulse density that is indicative of acceleration.